

# LZ2424J

## 1/4 type B/W CCD Area Sensor for CCIR

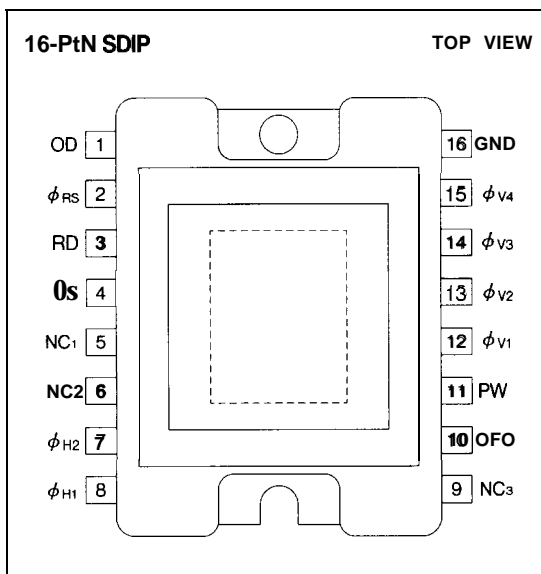
### DESCRIPTION

LZ2424J is a 1/4-type (4.5 mm) solid-state image sensor that consists of PN photo-diodes and CCDs (charge-coupled devices). Having approximately 320000 pixels (horizontal 542 X vertical 582), the sensor provides a high resolution stable B/W image.

### FEATURES

- Number of pixels :512 (H) X 582 (V)  
Pixel pitch : 7.2  $\mu\text{m}$  (H) X 4.7  $\mu\text{m}$  (V)  
Number of optical black pixels  
: Horizontal; front 2 and rear 28
- Low fixed pattern noise and lag
- No burn-in and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Variable electronic shutter (1/50 to 1/1 0 000 s)
- Compatible with CCIR standard
- Package : 16-pin SDIP [CERDIP] (WDIP016-N-0500B)

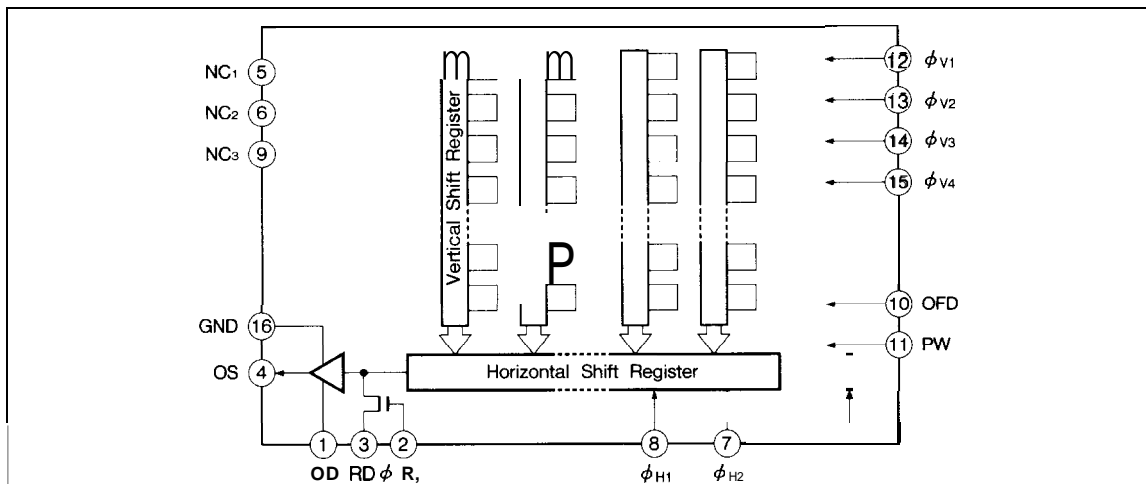
### PIN CONNECTIONS



CCD AREA SENSORS

2

### BLOCK DIAGRAM



## PIN DESCRIPTION

SYMBOL	PIN NAME
RD	Reset transistor drain
OD	Output transistor drain
Os	Video output
$\phi_{RS}$	Reset transistor clock
$\phi_{V1}, \phi_{V2}, \phi_{V3}, \phi_{V4}$	Vertical shift register clock
$\phi_{H1}, \phi_{H2}$	Horizontal shift register clock
OFD	Overflow drain
PW	P type well
GND	Ground
NC1, NC2, NC3	No connection

## ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

PARAMETER	SYMBOL	RATING	UNIT
Output transistor drain voltage	V <sub>OD</sub>	0 to +18	V
Reset drain voltage	V <sub>RD</sub>	0 to +18	v
Overflow drain voltage	V <sub>OM</sub>	0 to +55	v
Reset gate clock voltage	V $\phi_{RS}$	-0.3 to +18	v
Vertical shift register clock voltage	V $\phi_V$	-9.0 to +18	v
Horizontal shift register clock voltage	V $\phi_H$	-0.3 to +18	v
Voltage difference between PW and vertical clock	V <sub>PW</sub> - V $\phi_V$	-28 to 0	V
Storage temperature	T <sub>stg</sub>	-20 to +80	°C
Operating ambient temperature	T <sub>opr</sub>	-20 to +70	°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Operating ambient temperature		Topr		25.0		°C	
Output transistor drain voltage		VOD	14.5	15.0	16.0	v	
Reset transistor drain voltage		V <sub>RD</sub>		V <sub>OD</sub>		v	
Overflow drain voltage	When DC is applied	V <sub>OFD</sub>	5.0		19.0	v	1
	When pulse is applied p-p level	V <sub>φOFD</sub>	23.0			v	2
Ground		GND		0.0		v	
P-well voltage		V <sub>PW</sub>	- 10.0		V <sub>φVL</sub>	v	
Vertical shift register clock	LOW level	V <sub>φV1L</sub> , V <sub>φV3L</sub> V <sub>φV2L</sub> , V <sub>φV4L</sub>	- 8.5	- 8.0	-7.5	v	
	INTERMEDIATE level	V <sub>φV1I</sub> , V <sub>φV3I</sub> V <sub>φV2I</sub> , V <sub>φV4I</sub>		0.0		v	
	HIGH level	V <sub>φV1H</sub> , V <sub>φV3H</sub>	17.0	17.5	18.0	v	
Horizontal shift register clock	LOW level	V <sub>φH1L</sub> , V <sub>φH2L</sub>	- 0.05	0.0	0.05	v	
	HIGH level	V <sub>φH1H</sub> , V <sub>φH2H</sub>	4.7	5.0	6.0	v	
Reset gate clock	LOW level	V <sub>φRSL</sub>	0.0		V <sub>OO</sub> -13.0	v	
	HIGH level	V <sub>φRSH</sub>	V <sub>OD</sub> - 8.5		10.0	v	
Vertical shift register clock frequency		f <sub>φV1</sub> , f <sub>φV2</sub> f <sub>φV3</sub> , f <sub>φV4</sub>		15.63		kHz	
Horizontal shift register clock frequency		f <sub>φH1</sub> , f <sub>φH2</sub>		9.66		MHz	
Reset gate clock frequency		f <sub>φRS</sub>		9.66		MHz	

\* Connect NC 1, NC2 and NC3 to GND directly or through a capacitor larger than 0.047 μF.

## NOTES :

1. When DC voltage is applied, shutter speed is 1 /50 seconds.
2. When pulse is applied, shutter speed is less than 1/50 seconds.

## ELECTRICAL CHARACTERISTICS (Drive method : Field Accumulation)

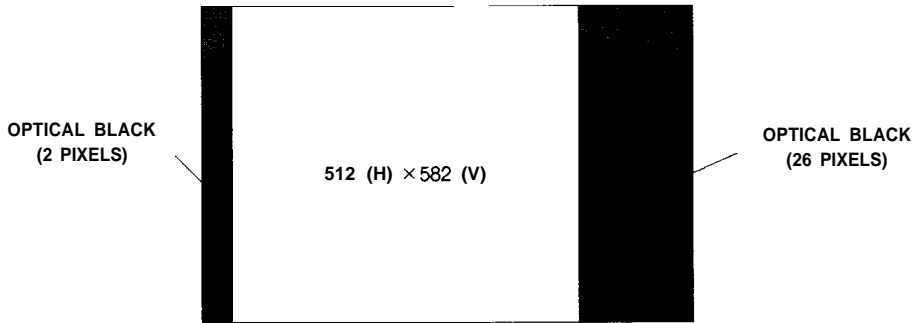
(Ta= 25°C, Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mmt))

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Standard output voltage	Vo		150		mV	2
Photo response non-uniformity	PRNU			15	%	3, 4
Saturation output voltage	Vaat	650			mV	3, 5
Dark output voltage	Vdark		0.5	3.0	mV	1, 6
Dark signal non-uniformity	DSNU		0.5	2.0	mV	1, 3, 7
Sensitivity	R	230	320		mV	8
Smear ratio	SMR		- 80	- 72	dB	9, 10
Image lag	AI			1.0	%	11
Blooming suppression ratio	ABL	1000				9, 12
Output transistor drain current	I <sub>OD</sub>		4.0	8.0	mA	
Output impedance	Ro		350		Ω	

## NOTES :

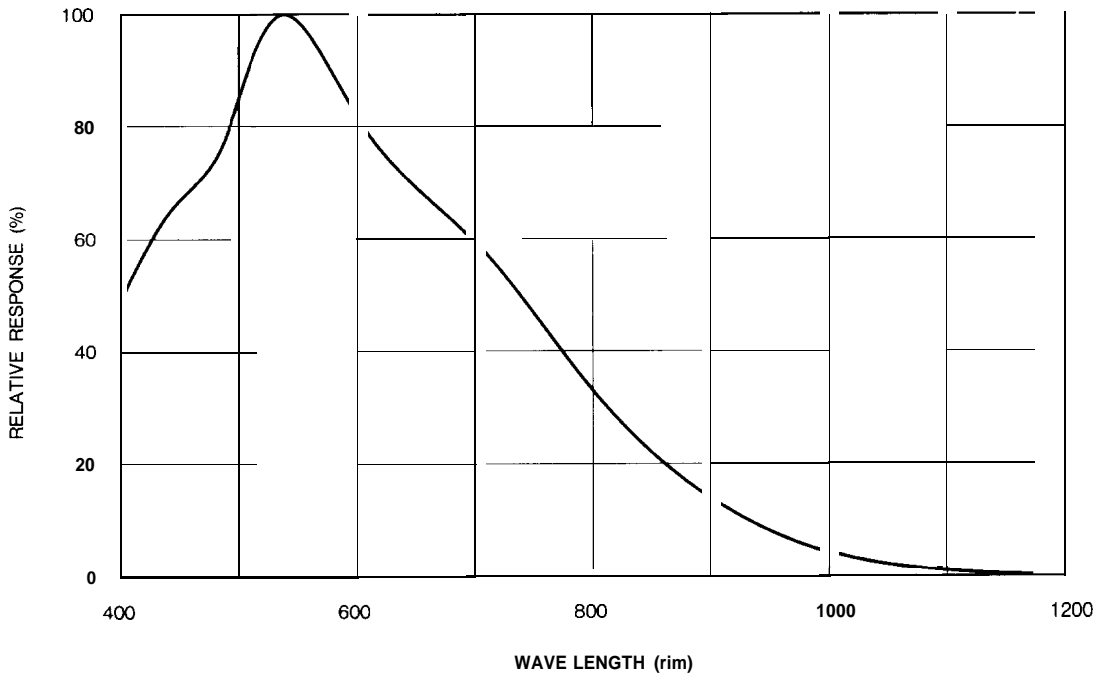
- Ta : +60°C
- The average output voltage under the uniform illumination. The standard exposure condition is defined when Vo is 150 mV.
- The image area is divided into 10X 10 segments. The segment's voltage is the average output voltage of all the pixels within the segment.
- PRNU is defined by  $(V_{max} - V_{min})/V_o$ , where Vmax and Vmin are the maximum and the minimum values of each segment's voltage respectively, under the standard exposure condition.
- The minimum segment's voltage under 10 times exposure of the standard exposure condition.
- The average output voltage under the non-exposure condition.
- DSNU is defined by  $(V_{dmax} - V_{dmin})$ , where Vdmax and Vdmin are the maximum and the minimum values of each segment's voltage respectively, under the non-exposure condition.
- The average output voltage when a 1 000lux light source with a 90% reflector is imaged with a lens at F4, f5D mm.
- The sensor is exposed only in the central area of V/I O square, where V is the vertical image size.
- SMR is defined by the ratio of the smear voltage detected during the vertical blanking period to the maximum output voltage in the V/I O square, with a lens at F4.
- The sensor is exposed at the exposure level corresponding to the standard condition. AI is defined by the ratio of the lag voltage measured at the 1st field during the non-exposure period to the standard output voltage.
- ABL is defined by the ratio of the exposure at the standard condition to the exposure at a point where a blooming is observed.

PIXEL STRUCTURE



CCD AREA SENSORS  
**2**

SPECTRAL RESPONSE EXAMPLE

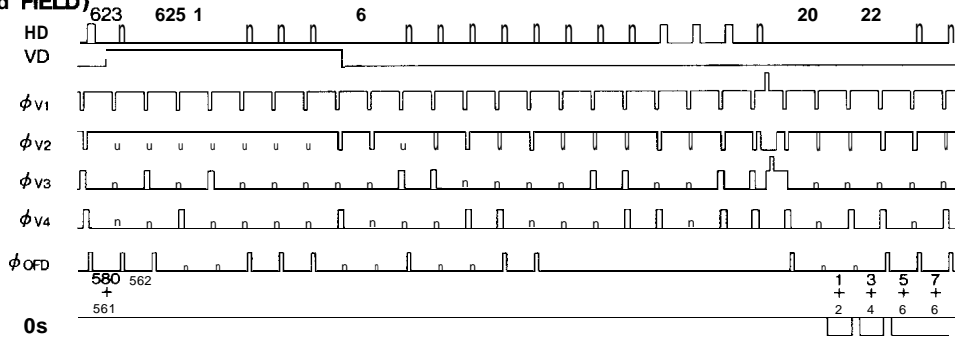


TIMING DIAGRAM EXAMPLE

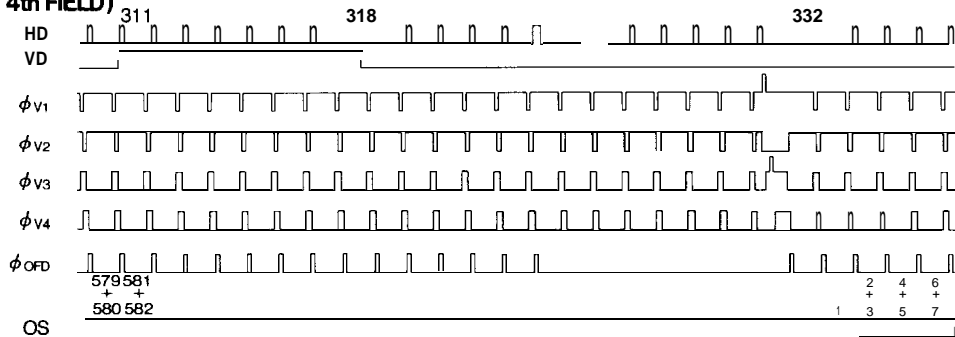
VERTICAL TRANSFER TIMING

Shutter speed  
1/2000 s

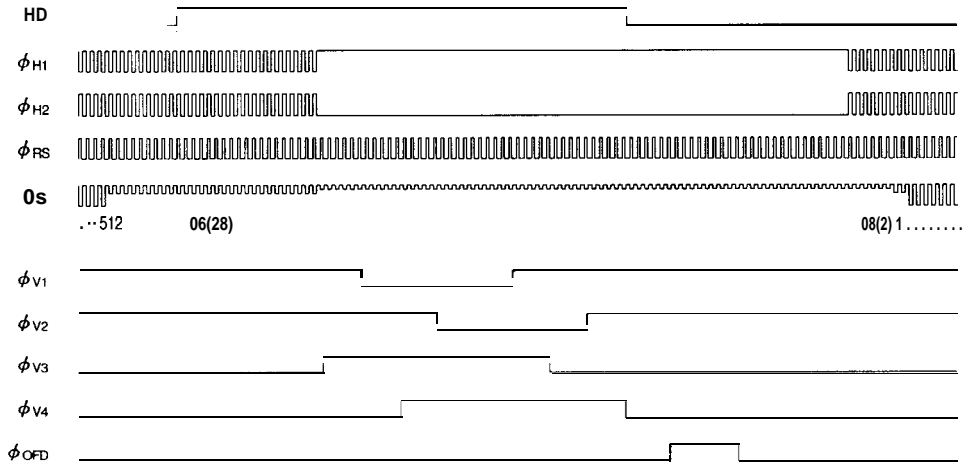
(1\*, 3rd FIELD)



(2nd, 4th FIELD)

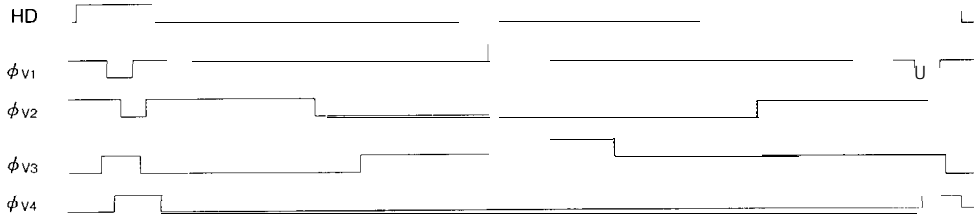


HORIZONTAL TRANSFER TIMING

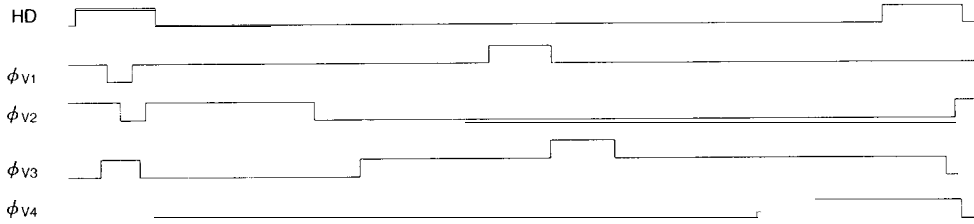


READOUT TIMING

(1st, 3rd FIELD)



(2nd, 4th FIELD)



SYSTEM CONFIGURATION EXAMPLE

